METHODS FOR FORMING INTEGRATED CIRCUIT DEVICES THROUGH SELECTIVE ETCHING OF AN INSULATION LAYER TO INCREASE THE SELF-ALIGNED CONTACT AREA ADJACENT A SEMICONDUCTOR REGION AND INTEGRATED CIRCUIT DEVICES FORMED THEREBY

Abstract of the Disclosure

Integrated circuit devices and methods of manufacturing same are disclosed in which an insulation layer is selectively etched to increase the self-aligned contact area adjacent a semiconductor region. For example, a pair of interconnection patterns may be formed on a substrate with the substrate having a semiconductor region disposed between the interconnection patterns. An etch-stop layer may then be formed on the pair of interconnection patterns and the substrate followed by the formation of a sacrificial insulation on the pair of interconnection patterns and on the semiconductor region. The sacrificial insulation layer is then selectively etched to expose portions of the etch-stop layer that extend on the surfaces of the pair of interconnection patterns. Sidewall insulation spacers, which are made of a different material than the sacrificial insulation layer, may then be formed on sidewall portions of the pair of interconnection patterns in an upper gap region between the interconnection patterns and on a portion of the sacrificial insulation layer covering the semiconductor region. The portion of the sacrificial insulation layer that covers the semiconductor region may then be selectively etched, using the sidewall insulation spacers as an etching mask, to define recesses underneath the sidewall insulation spacers.